N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} 40V
- I_D 80A
- $R_{DS(ON)}$(at V_{GS}=10V) 4.4mΩ
- $R_{DS(ON)}$(at V_{GS}=4.5V) 8mΩ
- 100% EAS Tested
- 100% V_{DS} Tested

General Description

- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor

■ Limiting Values

Parameter			Symbol	Min	Max	Unit
Drain-source Voltage			V_{DS}	-	40	V
Gate-source Voltage			V_{GS}	-20	20	V
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25 , V_{GS}= 10V	I_D	-	18	A
		T_A=100 , V_{GS}= 10V		-	12.7	
Continuous Drain Current (Note 1,3)	Steady-State	T_C=25 , V_{GS}= 10V, Chip limitation		-	80	
		T_C =100 , V_{GS}= 10V		-	56	
Pulsed Drain Current	T_C=25 , t 10μs		I_{DM}	-	320	A
Avalanche energy (non-repetitive)	V_G=10V, R_G=25Ω, L=0.5mH, IAS=15.5A		EAS	-	60	mJ
Total Power Dissipation (Note 1,2)	Steady-State	T_A=25	P_D	-	2.6	W
		T_A=100		-	1.3	
Total Power Dissipation (Note 1,3)	Steady-State	T_C=25		-	51	
		T_C =100		-	25	

■ Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	40	-	-	V
		V_{GS}= 0V, I_D=10mA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=32V, V_{GS}=0V	-	-	1	μA
		V_{DS}=32V, V_{GS}=0V, Tj=125	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	1.2	1.7	2.5	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=40A	-	3.3		mΩ
		V_{GS}=4.5V, I_D=20A	-	5.8	8	mΩ
Diode Forward Voltage	V_{SD}	I_S=40A, V_{GS}=0V	-	0.85	1.2	V

Gate resistance

Typical Electrical and Thermal Characteristics Diagrams

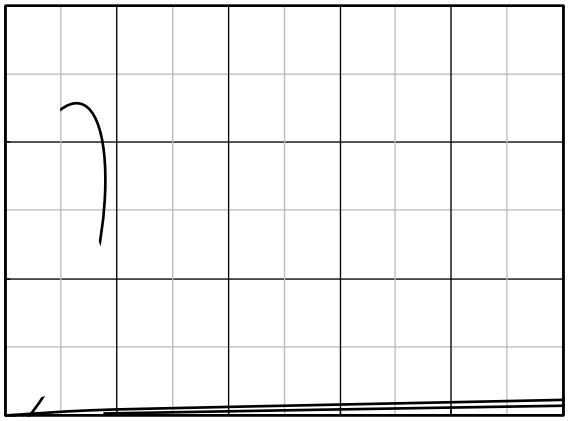


Figure 1. Output Characteristics

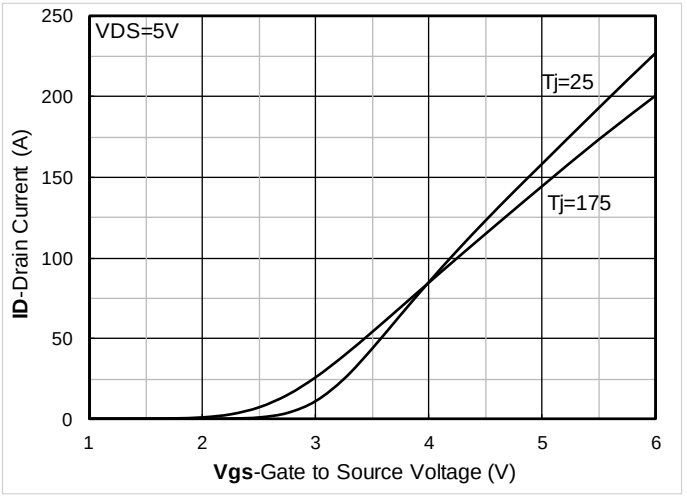


Figure 2. Transfer Characteristics

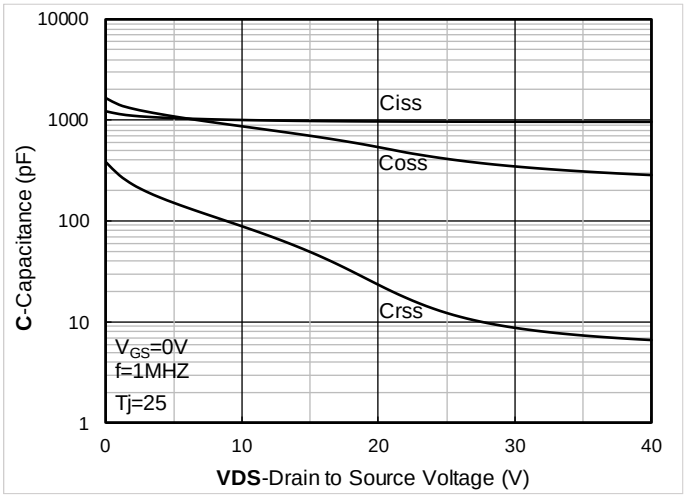


Figure 3. Capacitance Characteristics

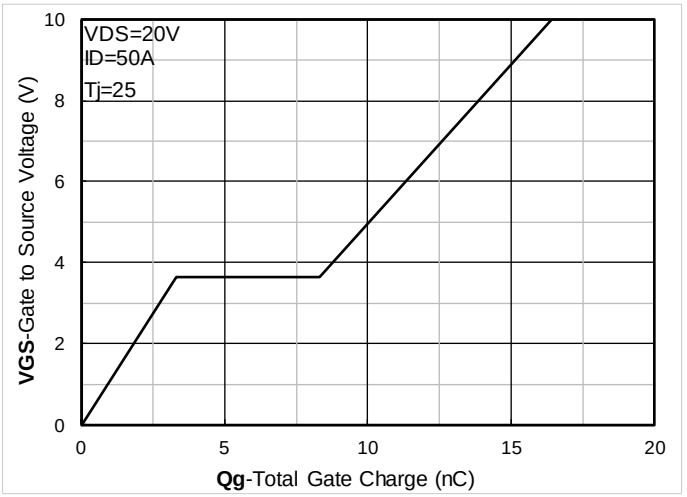
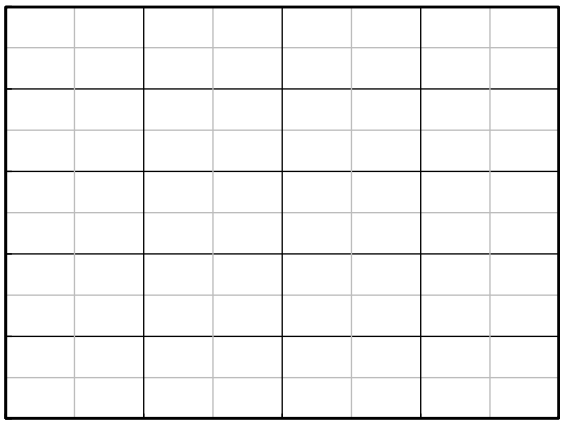


Figure 4. Gate Charge



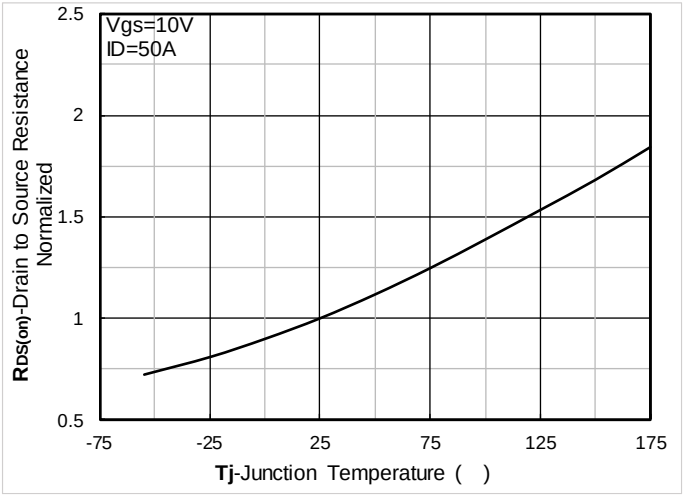


Figure 5. On-Resistance vs Gate to Source Voltage

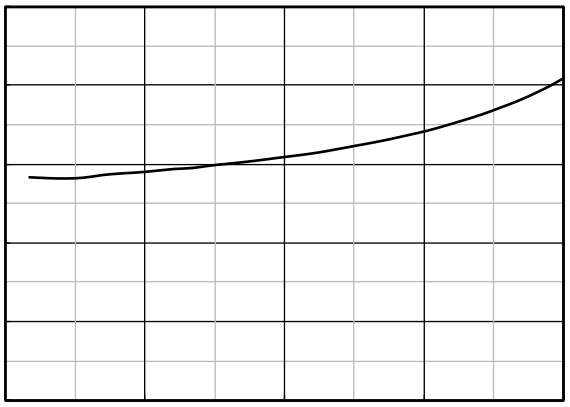


Figure 7. $R_{DS(on)}$ VS Drain Current

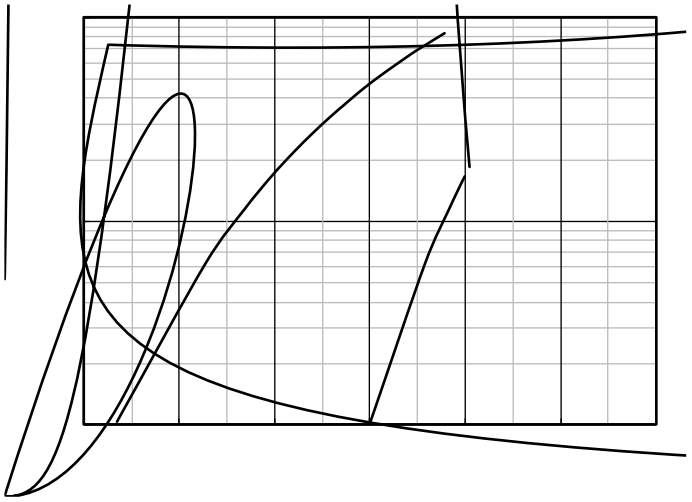


Figure 8. Forward characteristics of reverse diode

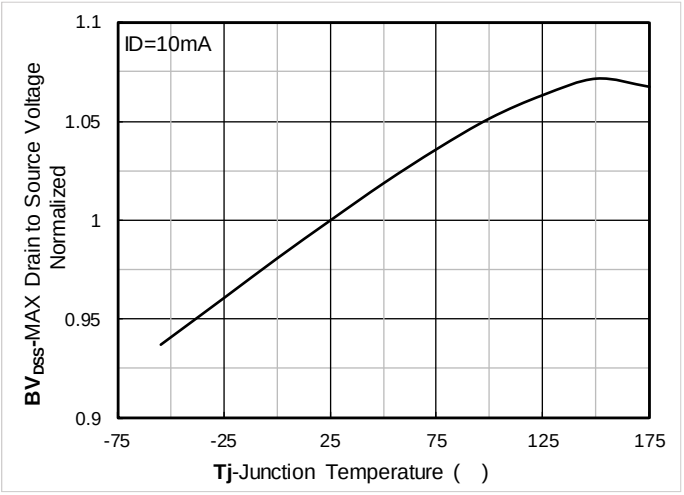


Figure 9. Normalized breakdown voltage

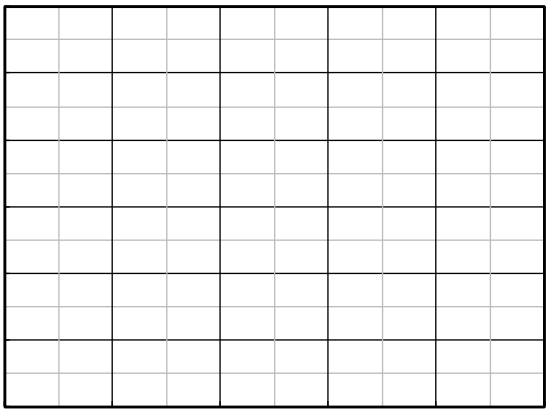
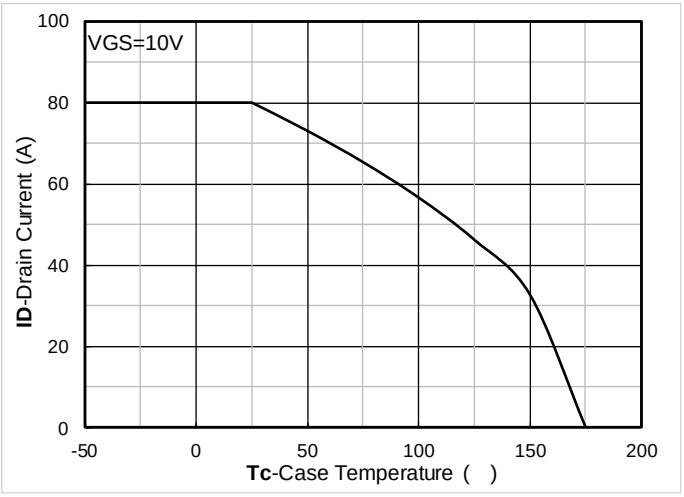


Figure 10. Normalized Threshold voltage



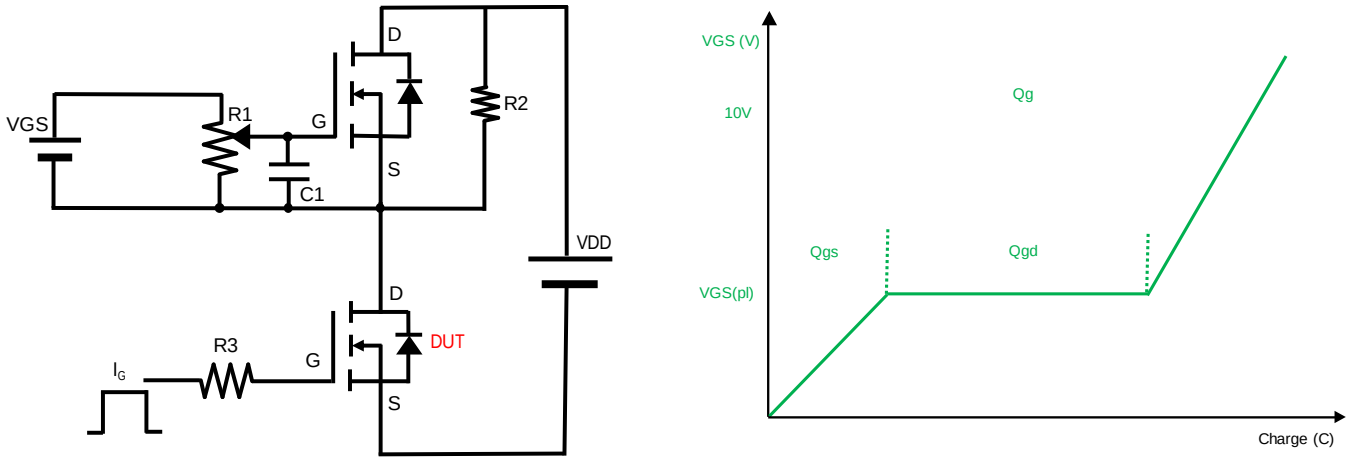


Figure B. Gate Charge Test Circuit & Waveform

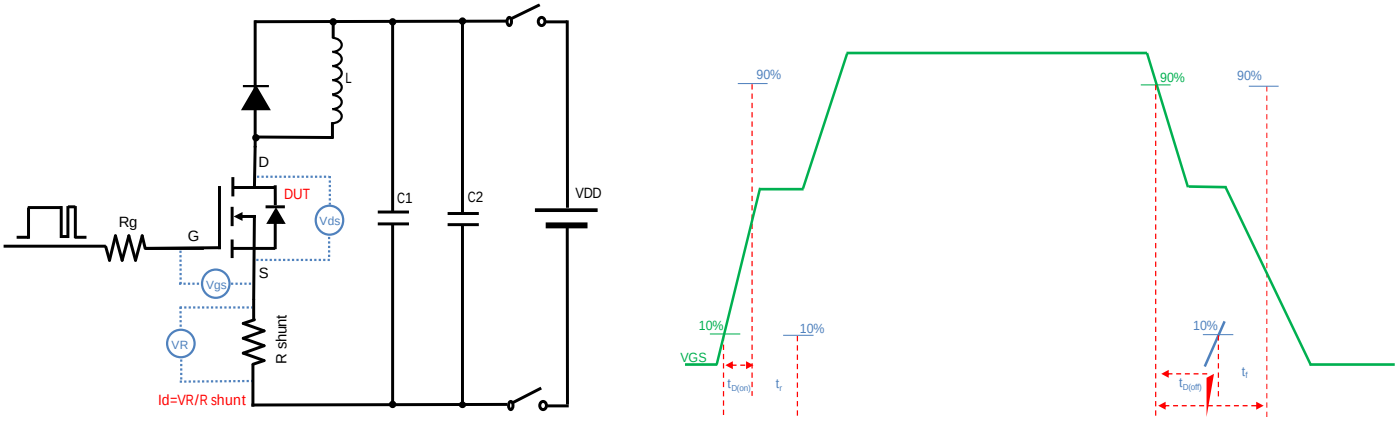


Figure C. Resistive Switching Test Circuit & Waveform

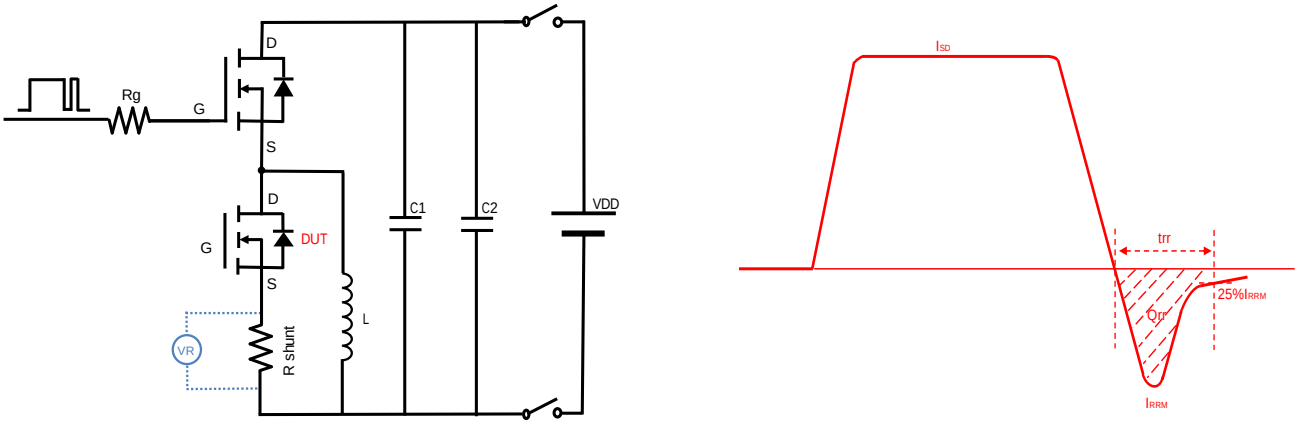


Figure D. Diode Recovery Test Circuit & Waveform