P-Channel Enhancement Mode Field Effect Transistor

Product Summary

ð V_{DS}	-80 V
ð I_D	-50 A
ð $R_{DS(ON)}$(at V_{GS}=-10V)	17 mq
ð $R_{DS(ON)}$(at V_{GS}=-6V)	19 mq
ð $R_{DS(ON)}$(at V_{GS}=-4.5V)	22 mq

ð 100% EAS Tested
ð 100% V_{DS} Tested

General Description

ð Split gate trench MOSFET technology
ð Low $R_{DS(on)}$ & FOM
ð Excellent stability and uniformity
ð Moisture Sensitivity Level 1
ð Epoxy Meets UL 94 V-0 Flammability Rating
ð Halogen Free

Applications

ð Power management
ð Portable equipment

y **Absolute Maximum Ratings**

y' Electrical Characteristics (T_J=25 unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=-250εA	-80	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=-80V, V_{GS}=0V	-	-	-1	εA
		V_{DS}=-80V, V_{GS}=0V, Tj=150	-	-	-100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±18V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=-250εA	-1.2	-2.1	-3	

Typical Electrical and Thermal Characteristics Diagrams

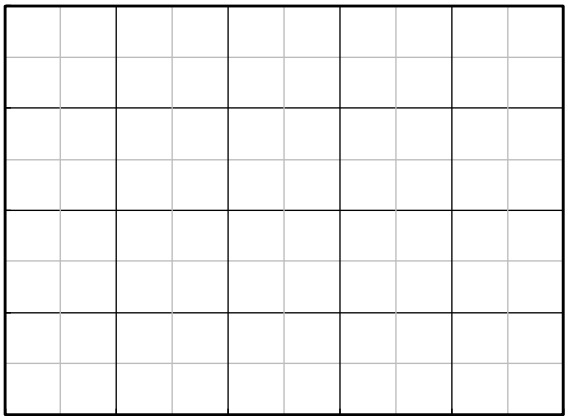

Figure 1. Output Characteristics

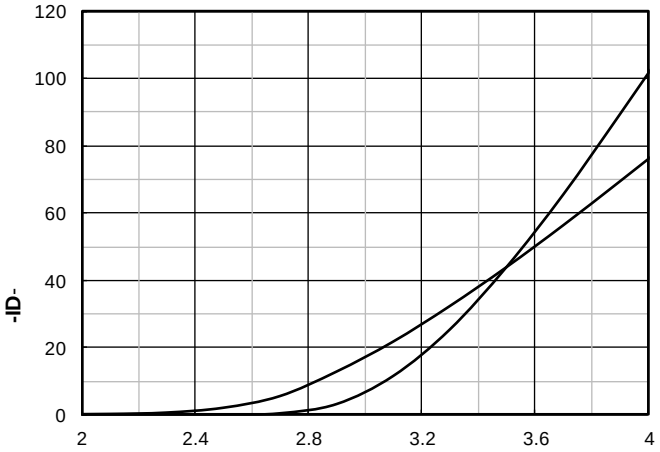

Figure 2. Transfer Characteristics

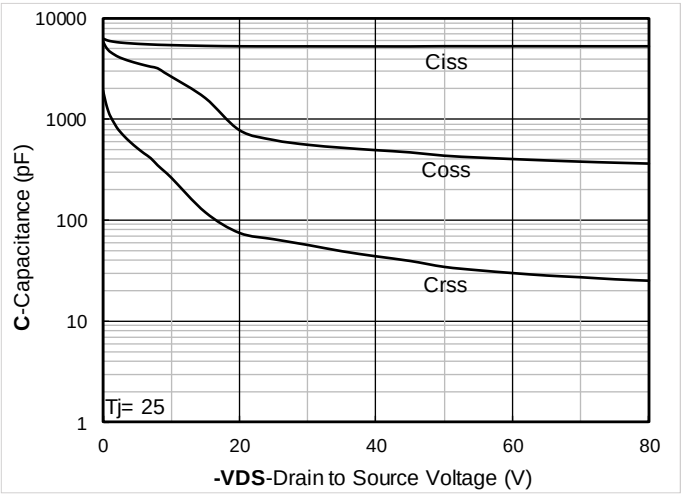

Figure 3. Capacitance Characteristics

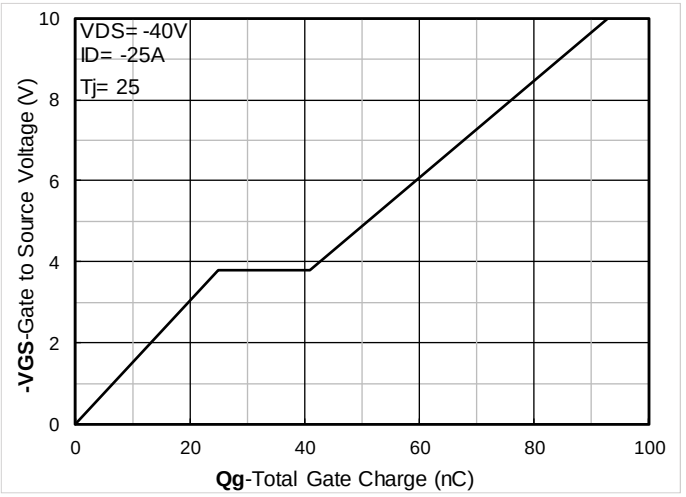

Figure 4. Gate Charge

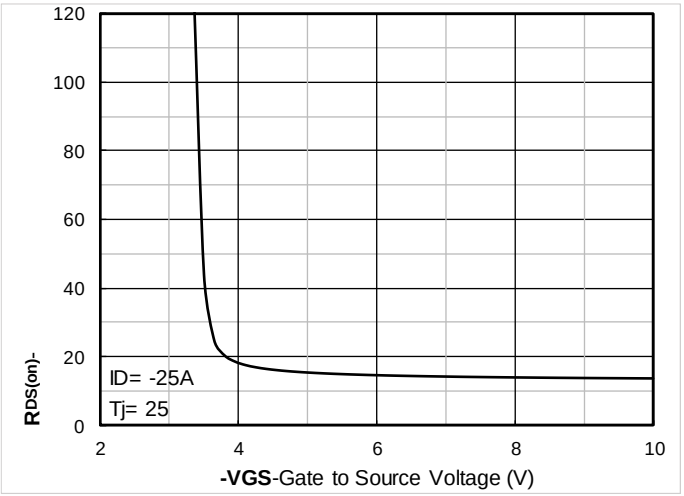

Figure 5. On-Resistance vs Gate to Source Voltage

Figure 6. Normalized On-Resistance

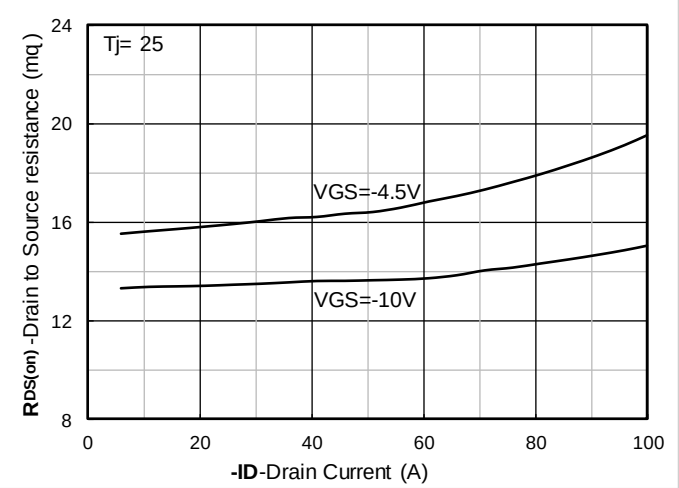

Figure 7. $R_{DS(on)}$ VS Drain Current

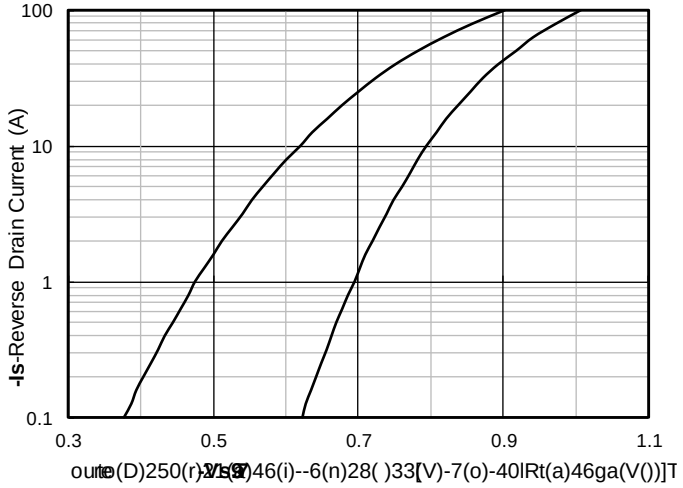

Figure 8. Forward characteristics of reverse diode

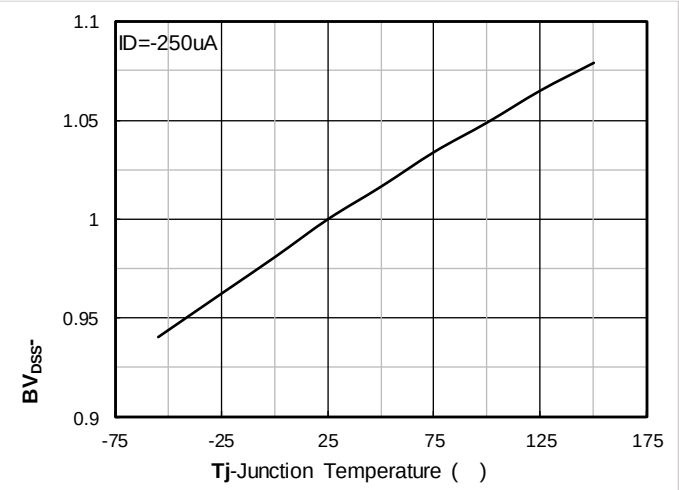

Figure 9. Normalized breakdown voltage

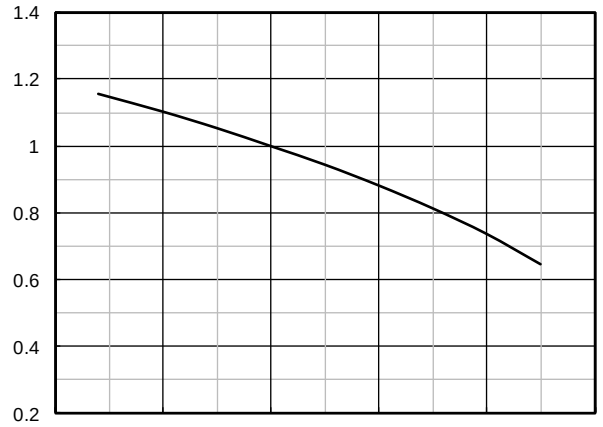

Figure 10. Normalized Threshold voltage

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