N-Channel Enhancement Mode Field Effect Transistor

Product Summary

- V_{DS} 40V
- I_D 69A
- $R_{DS(ON)}$(at V_{GS}=10V) 5.7mΩ
- 100% EAS Tested
- 100% V_{DS} Tested

General Description

- Split gate trench MOSFET technology
- Excellent package for heat dissipation
- High density cell design for low $R_{DS(ON)}$
- Moisture Sensitivity Level 1
- Epoxy Meets UL 94 V-0 Flammability Rating
- Halogen Free
- Part no. with suffix "Q" means AEC-Q101 qualified

Applications

- Power switching application
- Uninterruptible power supply
- DC-DC convertor
- 12V Automotive systems

■ Absolute Maximum Ratings (T_J=25 unless otherwise noted)

Parameter			Symbol	Limit	Unit
Drain-source Voltage			V_{DS}	40	V
Gate-source Voltage			V_{GS}	±20	V
Continuous Drain Current (Note 1,2)	Steady-State	T_A=25 , V_{GS}= 10V	I_D	15	A

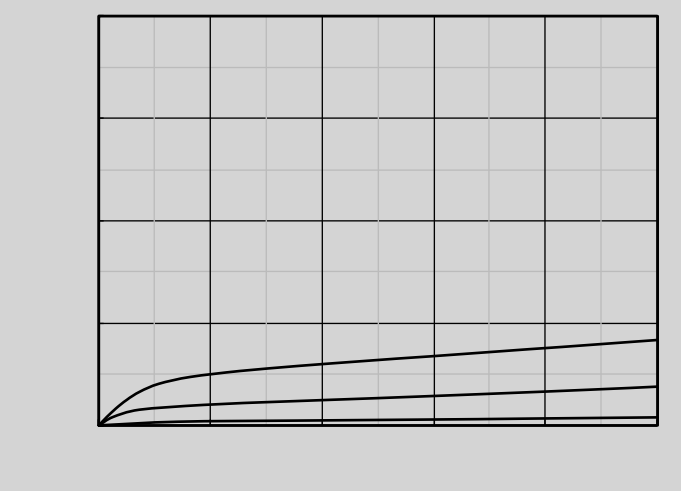
■ Electrical Characteristics (T_J=25 unless otherwise noted)

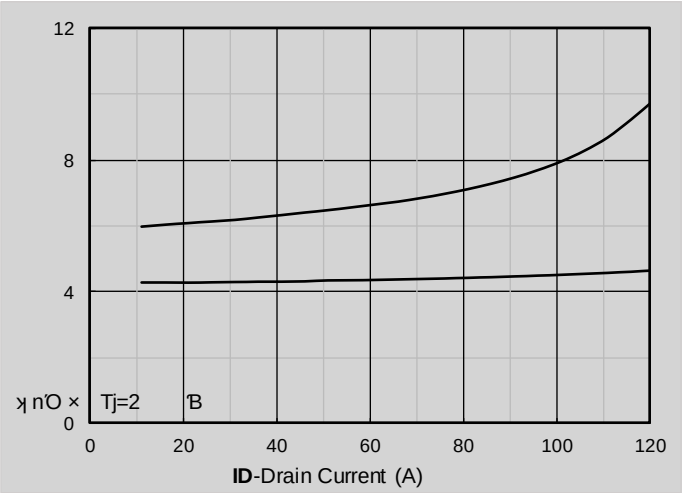
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Parameter						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}= 0V, I_D=250μA	40	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=40V, V_{GS}=0V	-	-	1	μA
		V_{DS}=40V, V_{GS}=0V, Tj=125	-	-	100	
Gate-Body Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	-	-	±100	nA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}= V_{GS}, I_D=250μA	2	3	4	V
Static Drain-Source On-Resistance	$R_{DS(ON)}$	V_{GS}=10V, I_D=20A	-	4.2	5.7	mΩ
Diode Forward Voltage	V_{SD}	I_S=20A, V_{GS}=0V	-	-	1.2	V
Gate resistance	R_G	f=1MHz	-	2	-	Ω
Maximum Body-Diode Continuous Current	I_S		-	-	69	A
Dynamic Parameters						
Input Capacitance	C_{iss}	V_{DS}=20V, V_{GS}=0V, f=1MHz	-	1080	-	pF
Output Capacitance	C_{oss}		-	460	-	
Reverse Transfer Capacitance	C_{rss}		-	3	-	
Switching Parameters						
Total Gate Charge	Q_g	V_{GS}=10V, V_{DS}=20V, I_D=30A	-	14.5	-	nC
Gate-Source Charge	Q_{gs}		-	5.2	-	
Gate-Drain Charge	Q_{gd}		-	3	-	
Reverse Recovery Charge	Q_{rr}	I_F=30A, di/dt=100A/us	-	49	-	nC
Reverse Recovery Time	t_{rr}		-	56	-	ns
Turn-on Delay Time	$t_{D(on)}$	V_{GS}=10V, V_{DD}=20V, I_D=30A R_{GEN}=2.2Ω	-	10	-	ns
Turn-on Rise Time	t_r		-	154	-	
Turn-off Delay Time	$t_{D(off)}$		-	15	-	
Turn-off fall Time	t_f		-	8	-	

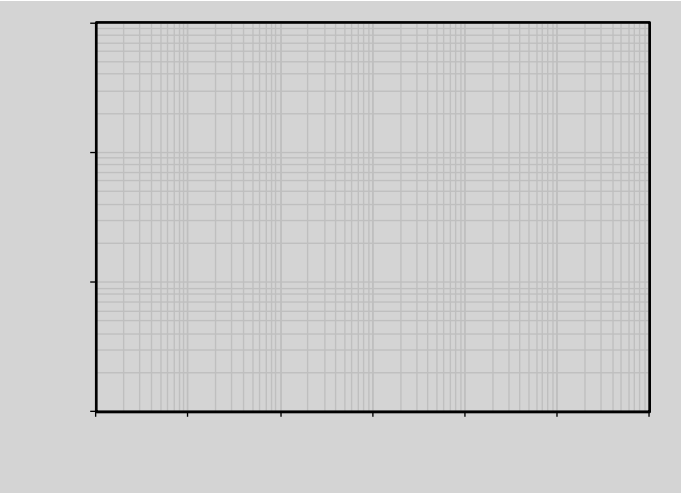
Note

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. The value of $R_{\theta JA}$ is measured with the device mounted on the 40mm*40mm*1.1mm single layer FR-4 PCB board with 1 in^2 pad of 2oz. Copper, in the still air environment with TA =25 .The maximum allowed junction temperature of 175 . The value in any given application depends on the user's specific board design.
3. Thermal resistance from junction to soldering point (on the exposed drain pad).

■Typical Electrical and Thermal Characteristics Diagrams




12
8
4
0
Tj=2
0
20
40
60
80
100
120
ID-Drain Current (A)



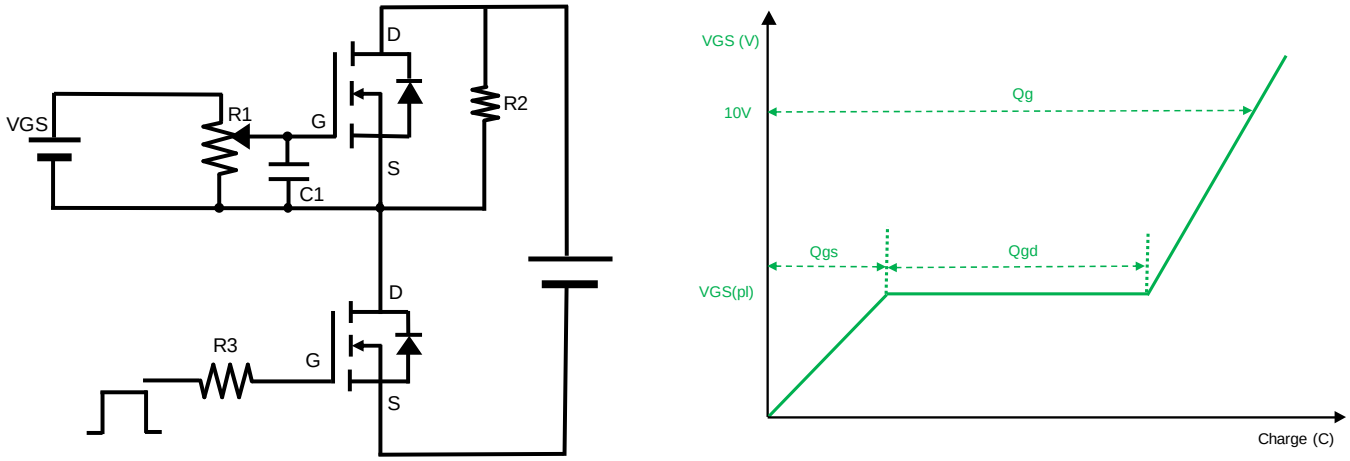
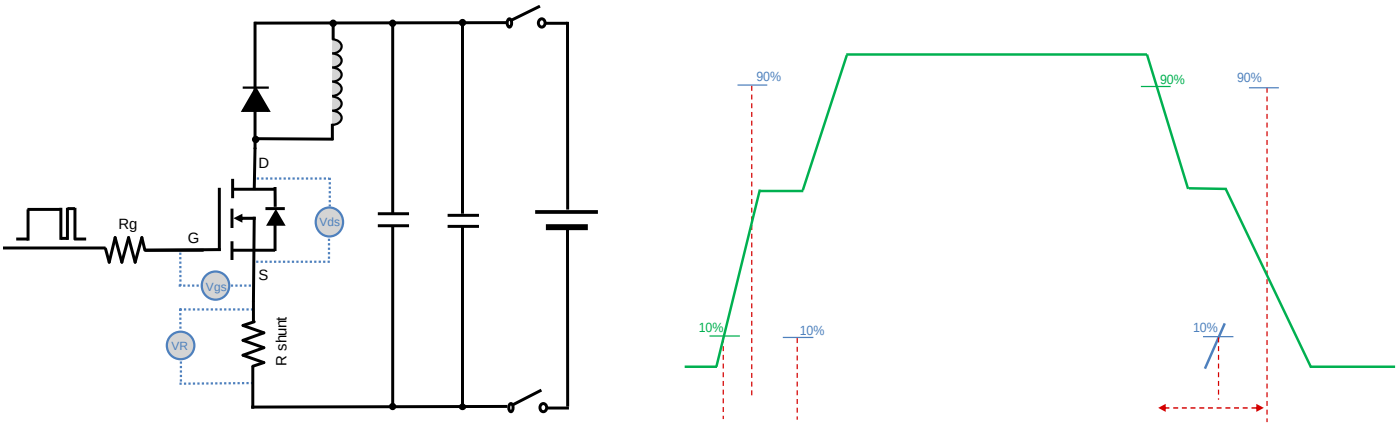
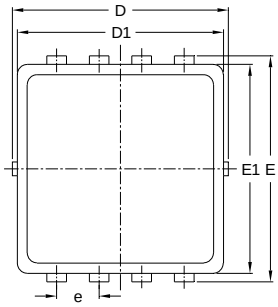


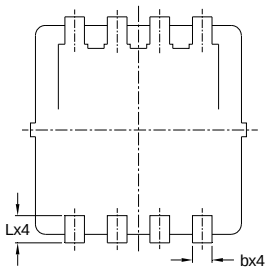
Figure B. Gate Charge Test Circuit & Waveform



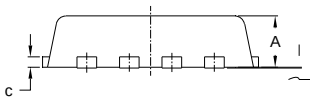
■ PDFN3333-8L-B-0.75MM Package information



TOP VIEW



BOTTOM VIEW



SIDE VIEW

UNIT mm

NOTE:
1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.
3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

SUGGESTED SOLDER PAD LAYOUT

Disclaimer

The information presented in this document is for reference only. M