# N-Channel Enhancement Mode Field Effect Transistor

## Product Summary

| | |
|---|---|
| $V_{DS}$ | 40V |
| $I_D$ | 340A |
| $R_{DS(ON)}$( at $V_{GS}$=10V) | 1.3m |
| 100% EAS Tested | |
| 100% $V_{DS}$ Tested | |

## General Description

Excellent package for heat dissipation
High density cell design for low $R_{DS(ON)}$
Moisture Sensitivity Level 1

**Electrical Characteristics** ($T_J$=25 unless otherwise noted)

| Parameter | Symbol | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Static Parameter** | | | | | | |
| Drain-Source Breakdown Voltage | $BV_{DSS}$ | $V_{GS}$= 0V, $I_D$ | 40 | - | - | V |
| | | $V_{GS}$= 0V, $I_D$=1mA | 40 | - | | |

## Typical Electrical and Thermal Characteristics Diagrams

Figure 1. Output Characteristics

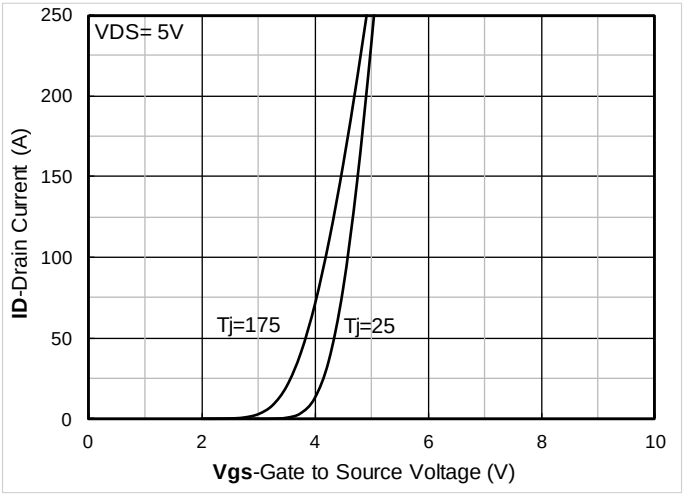



Figure 2. Transfer Characteristics

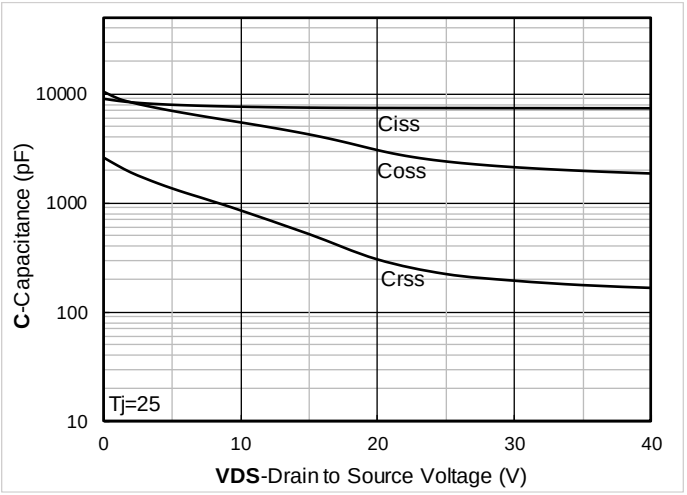



Figure 3. Capacitance Characteristics

Figure 4. Gate Charge

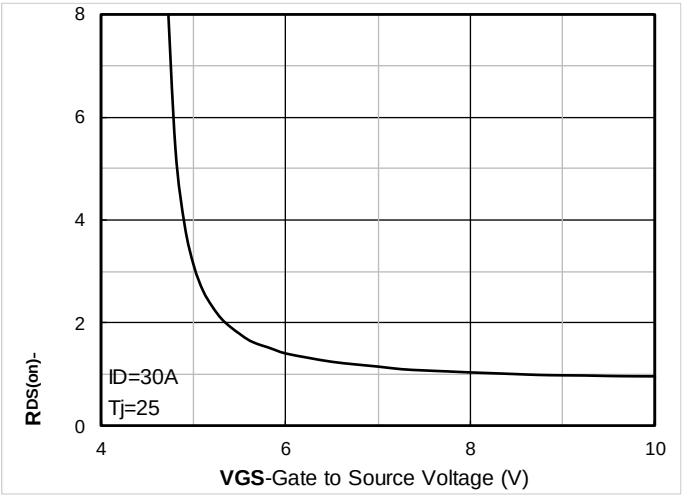



Figure 5. On-Resistance vs Gate to Source Voltage

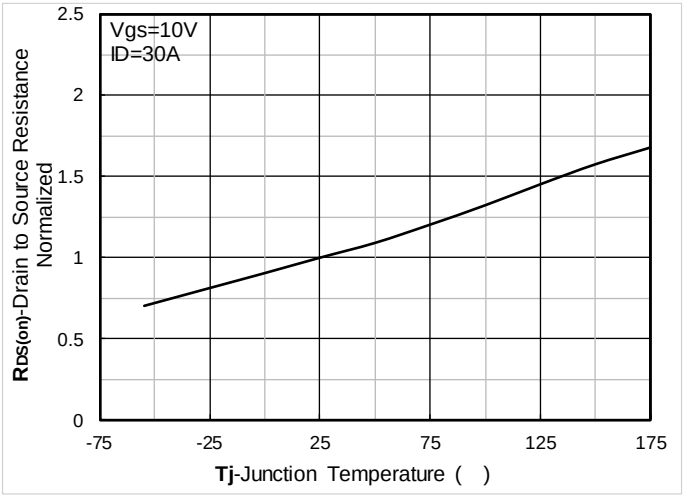
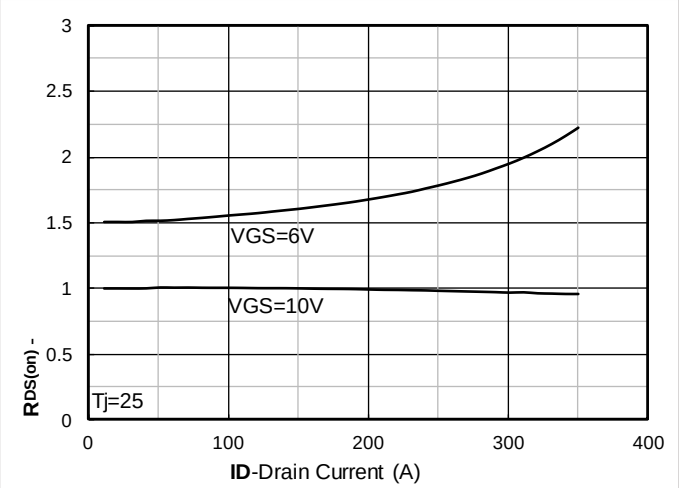



Figure 6. Normalized On-Resistance



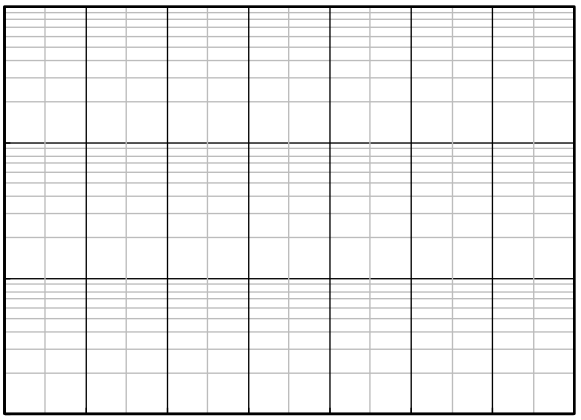



Figure 7. $R_{DS(on)}$

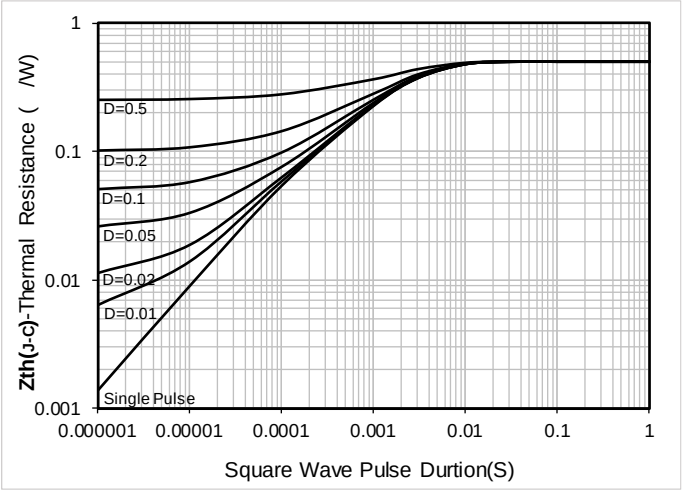



Figure 13. Maximum Transient Thermal Impedance

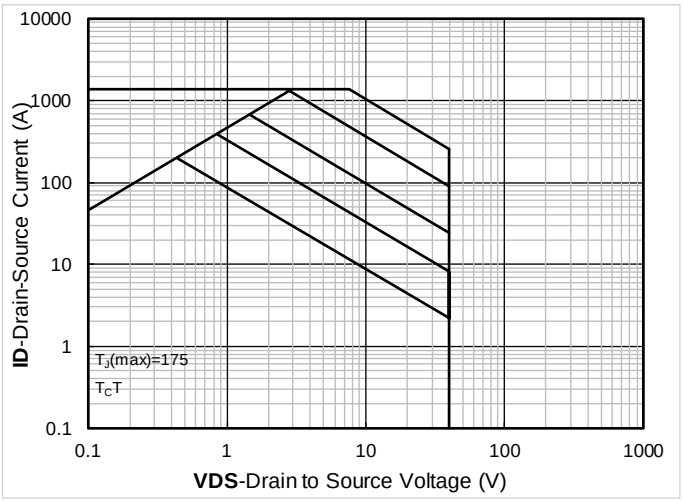



Figure 14. Safe Operation Area

## Test Circuits & Waveforms

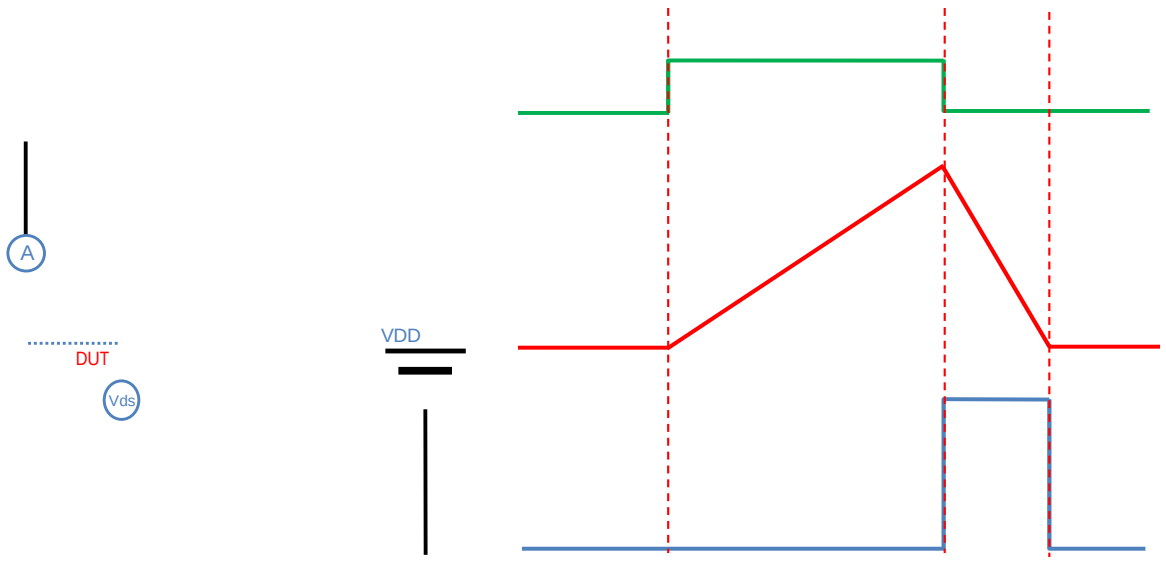



Figure A. Unclamped Inductive Switching (UIS) Test Circuit & Waveform

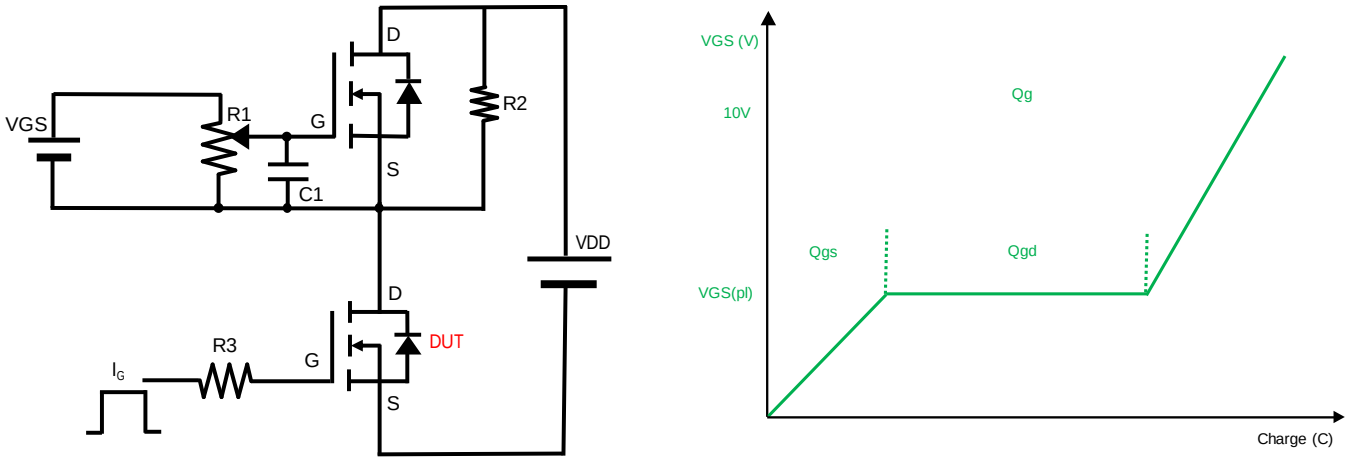



Figure B. Gate Charge Test Circuit & Waveform

## TOLL Package information

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | 2.2 | 2.3 | 2.4 |
| A1 | 1.7 | 1.8 | 1.9 |
| b | 0.7 | 0.8 | 0.9 |
| b1 | 9.7 | 9.8 | 9.9 |
| b2 | 1.1 | 1.2 | 1.3 |
| c | 0.4 | | |

Note:
1.Controlling dimension:in millimeters.
2.General tolerance:±0.03mm.
3.The pad layout is for reference purposes only.

SUGGESTED SOLDER PAD LAYOUT
TOP VIEW

## Disclaimer

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The product listed herein is designed to be used with automotive electronics,are not designed for use in medical, life-saving, lifesustaining,or